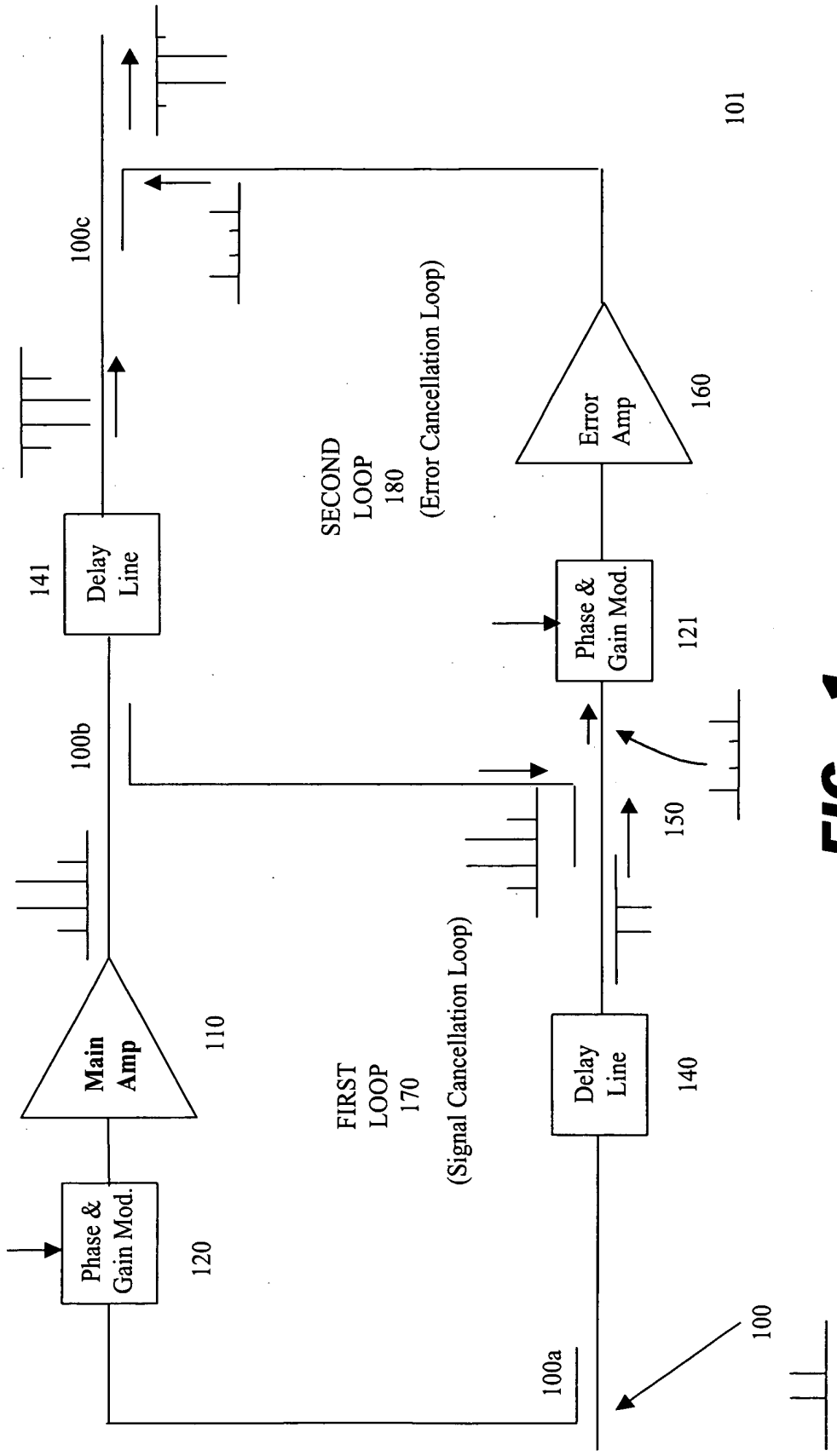


FIG. 1
PRIOR ART

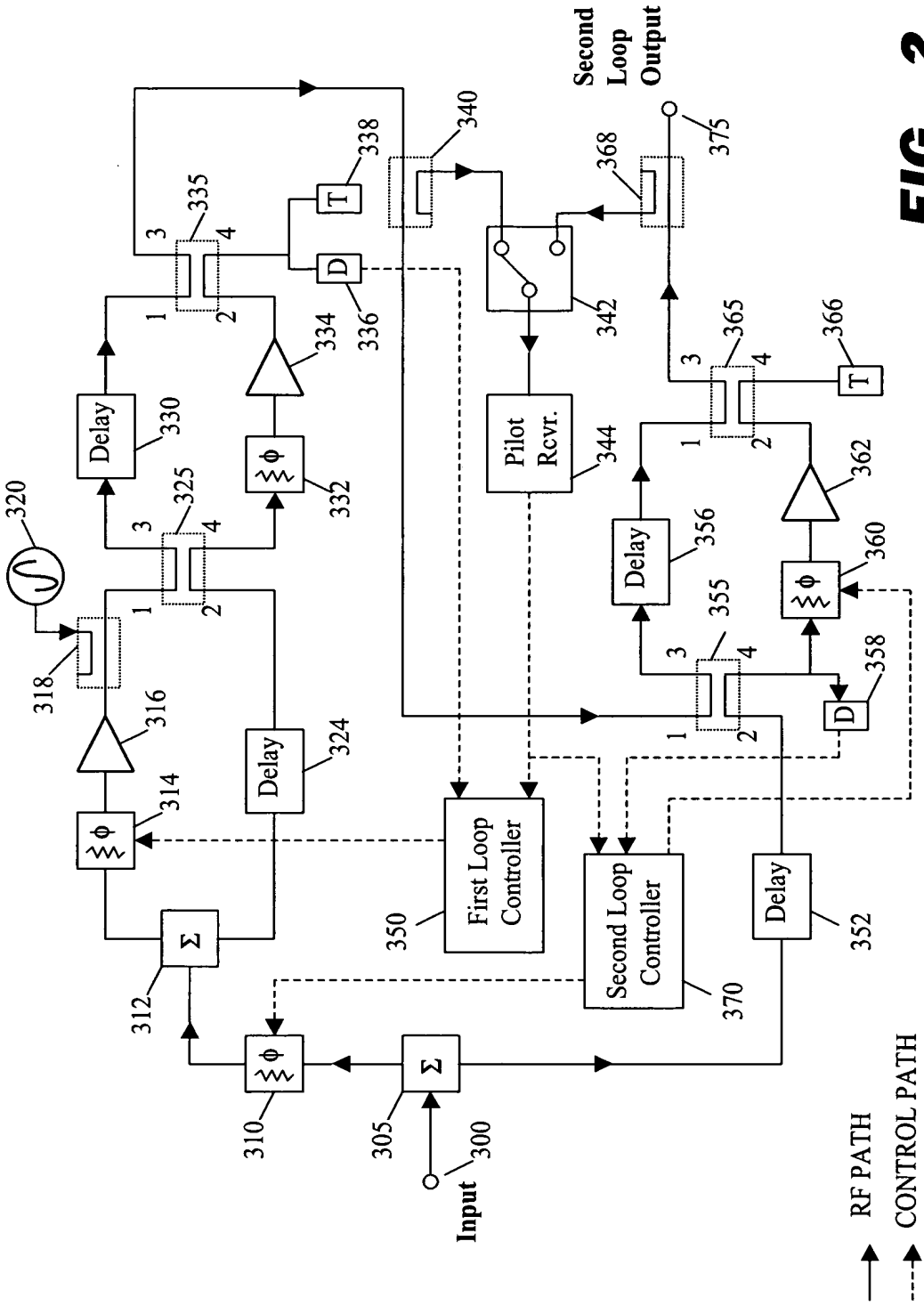


FIG. 2
PRIOR ART

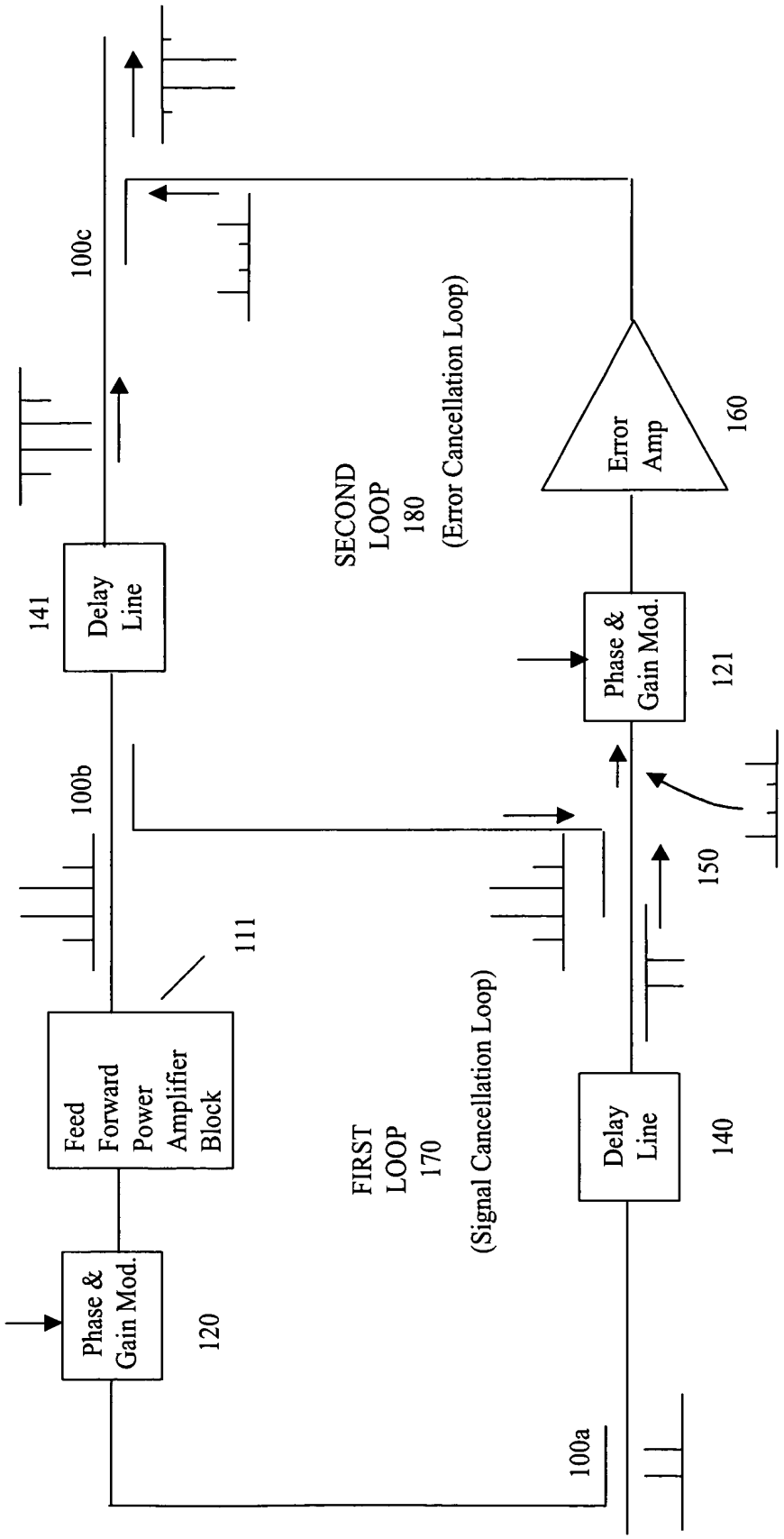
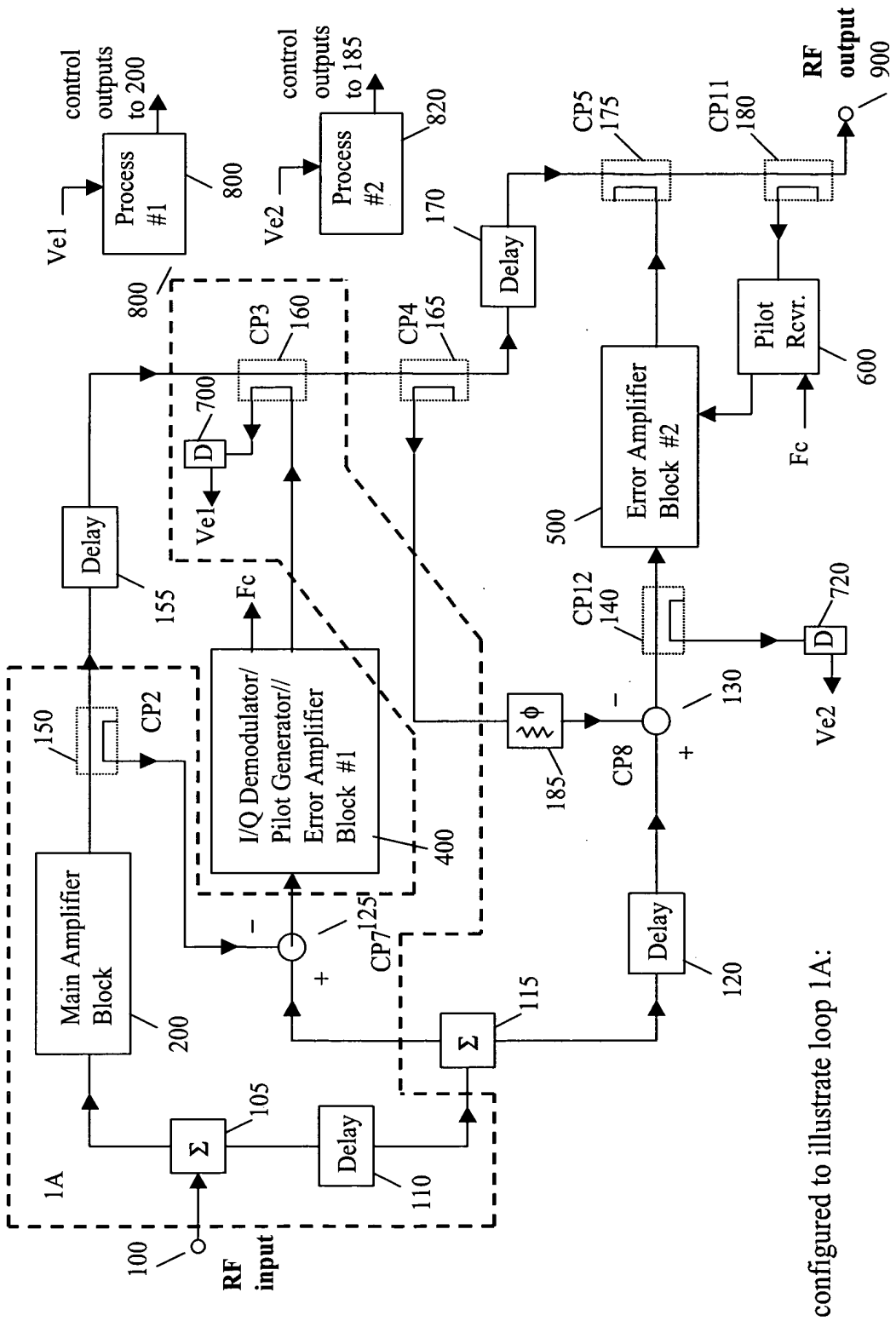


FIG. 3
PRIOR ART



configured to illustrate loop 1A:

FIG. 4

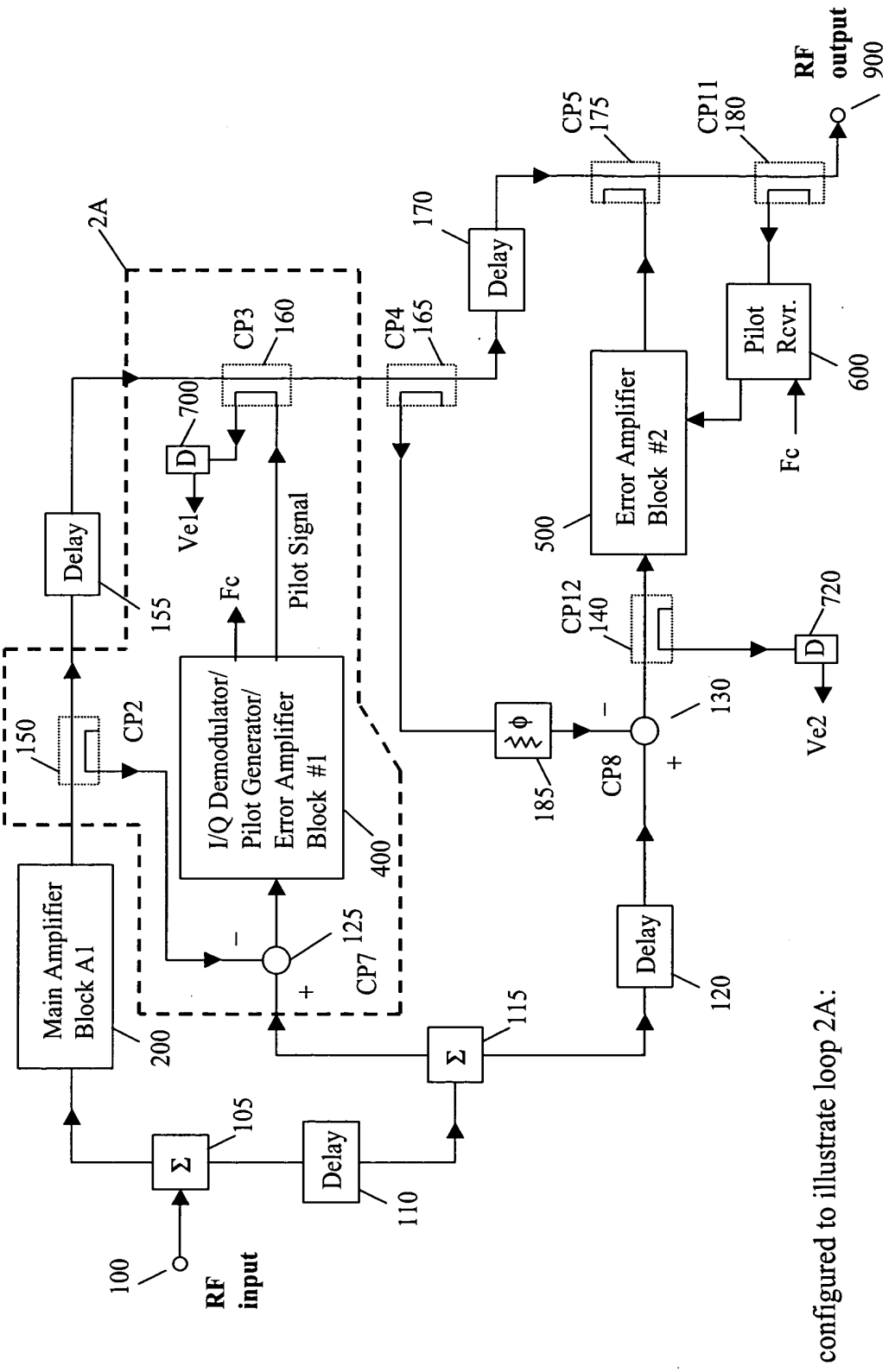


FIG. 5

configured to illustrate loop 2A:

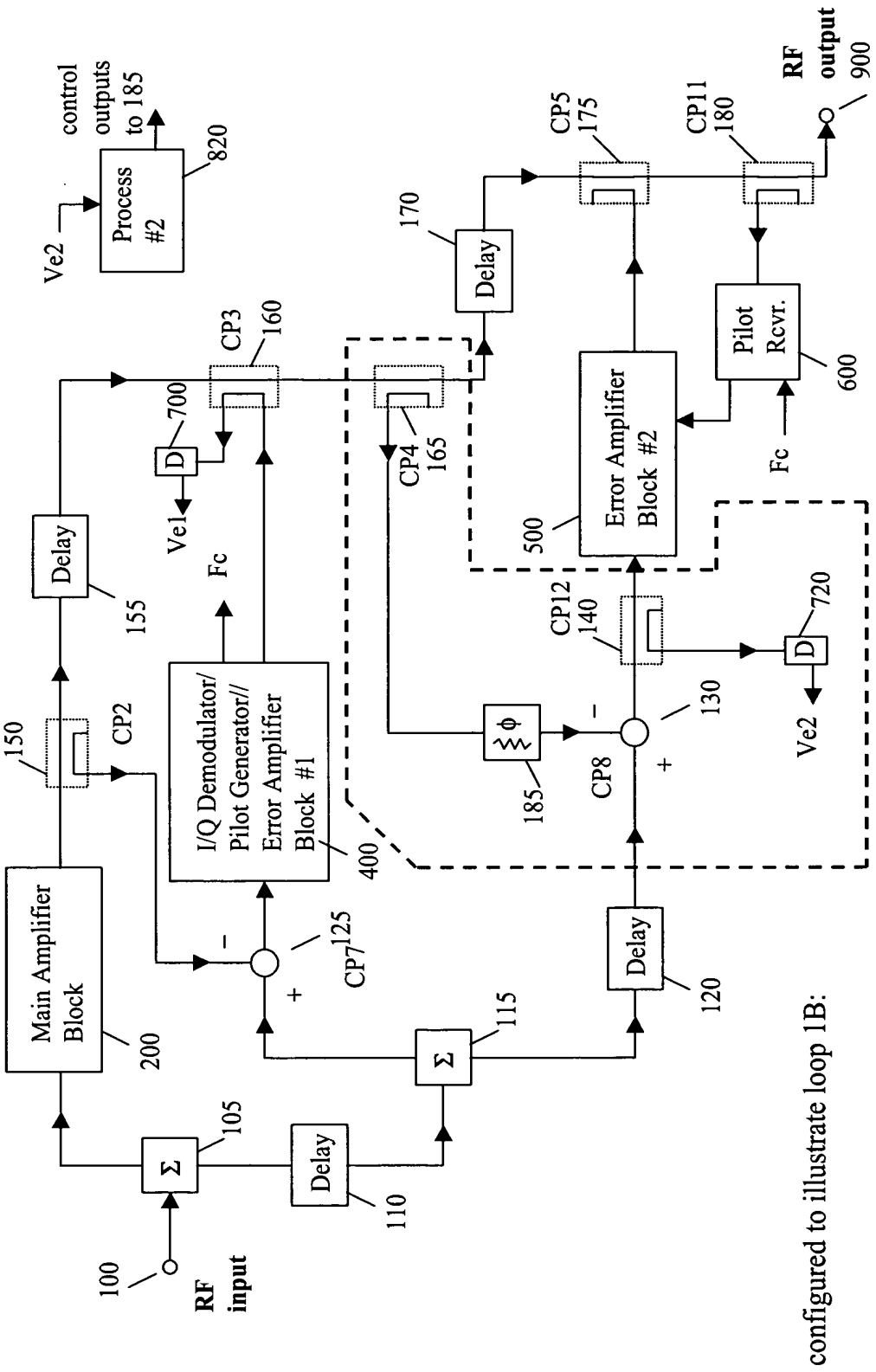
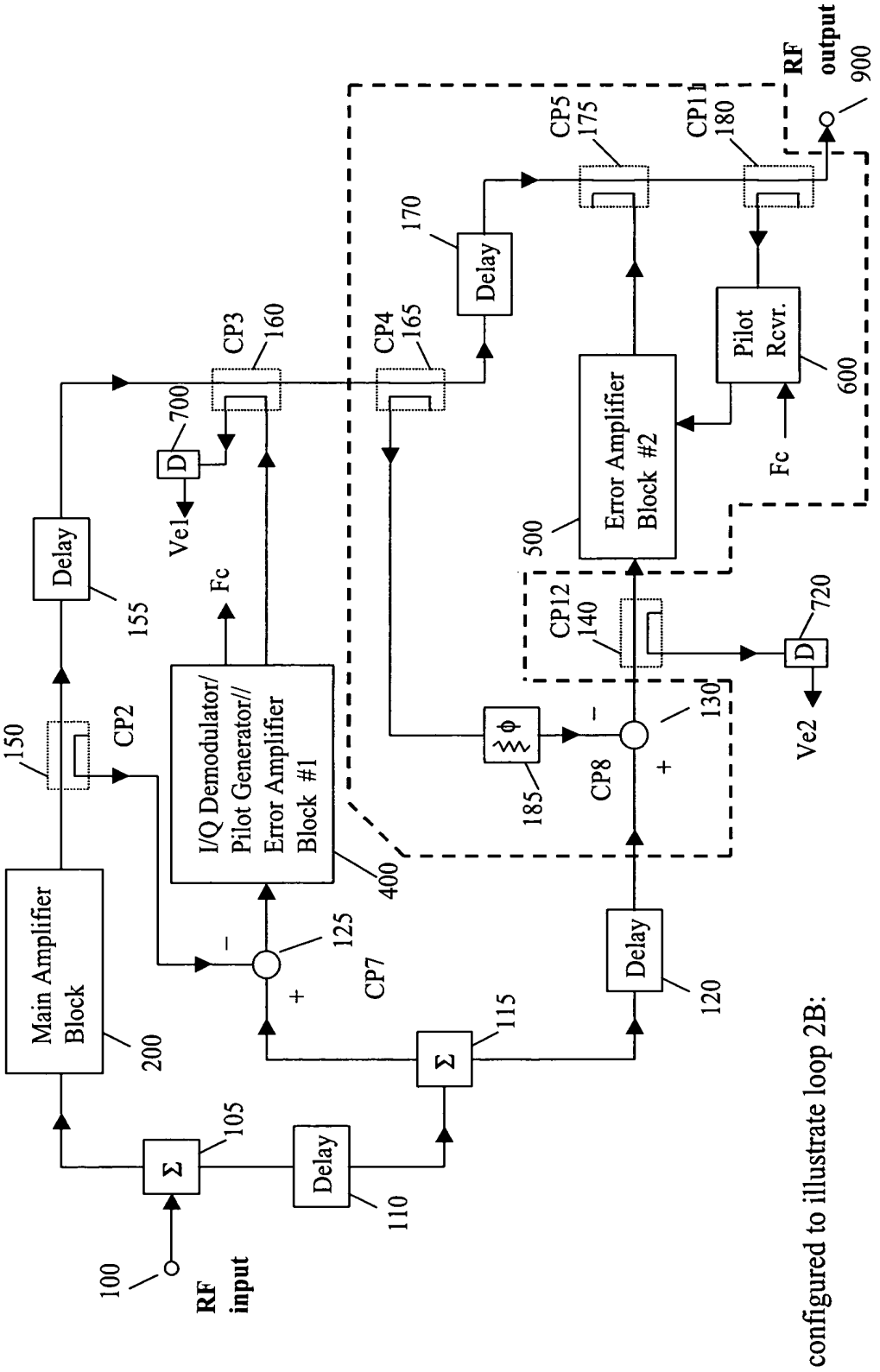


FIG. 6

configured to illustrate loop 1B:



configured to illustrate loop 2B:

FIG. 7

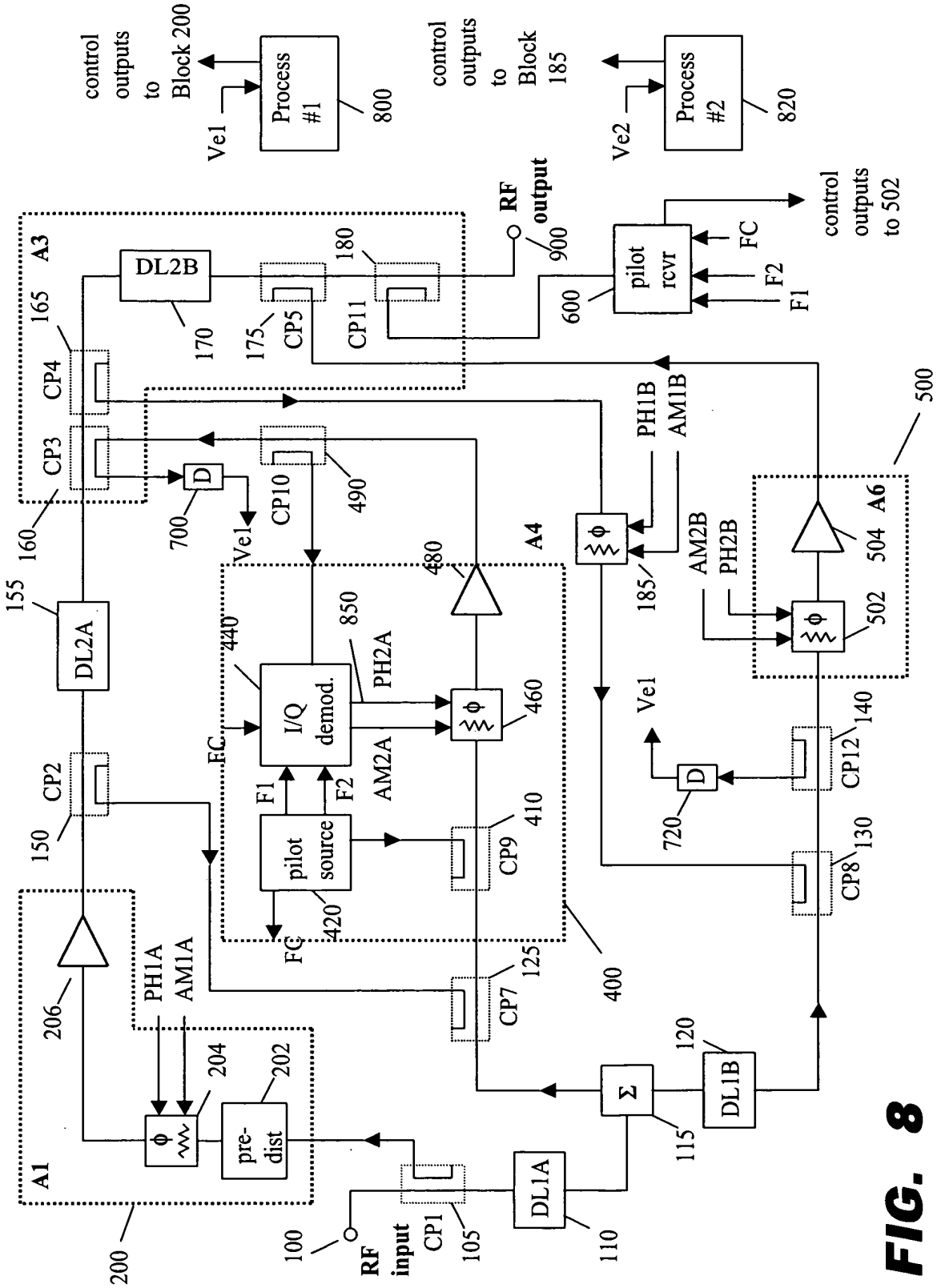

control outputs to Block 200
Process #1
800
Ve1
control outputs to Block 185
Process #2
820
Ve2
RF output
900
control outputs to 502
pilot rcvr
600
FC
F2
F1
A3
DL2B
170
165
CP4
175
CP5
180
CP11
CP3
160
700
D
Ve1
CP10
490
480
A4
155
DL2A
440
I/Q demod.
850
PH2A
460
FC
F1
F2
AM2A
150
CP2
pilot source
420
CP9
410
FC
125
CP7
400
PH1B
AM1B
185
AM2B
PH2B
A6
504
500
502
Ve1
720
D
CP12
140
CP8
130
206
PH1A
AM1A
204
202
pre-dist
A1
200
100
RF input
CP1
105
DL1A
110
Σ
115
120
DL1B

FIG. 8

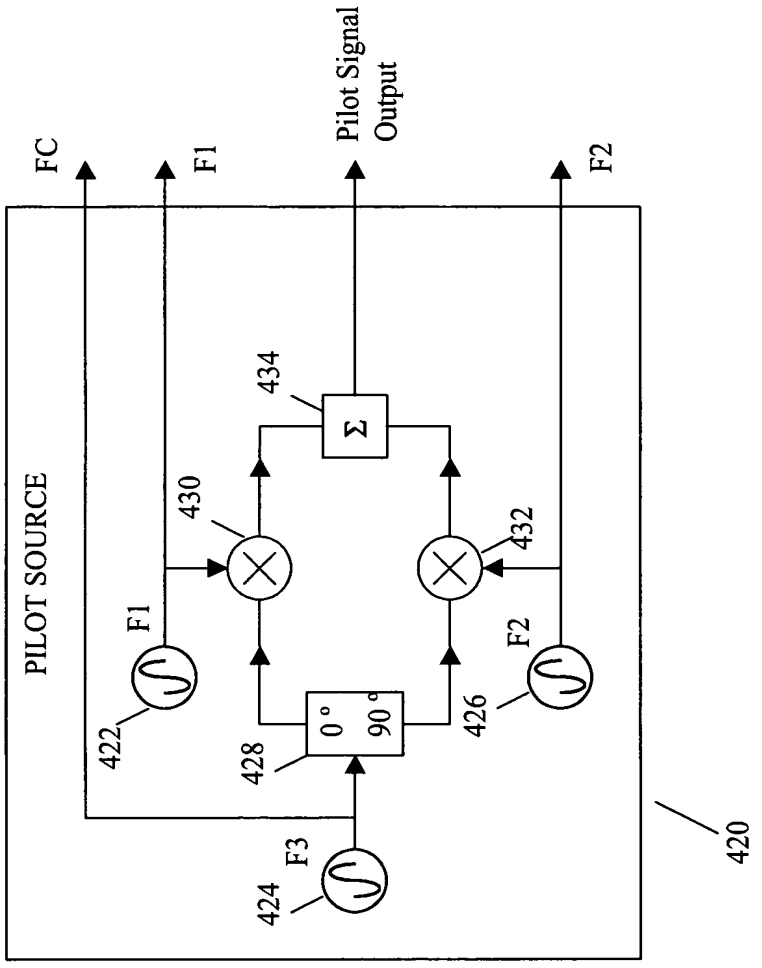

FC
F1
Pilot Signal Output
F2
PILOT SOURCE
434
Σ
430
432
F1
F2
422
426
428
0°
90°
F3
424
420

FIG. 9

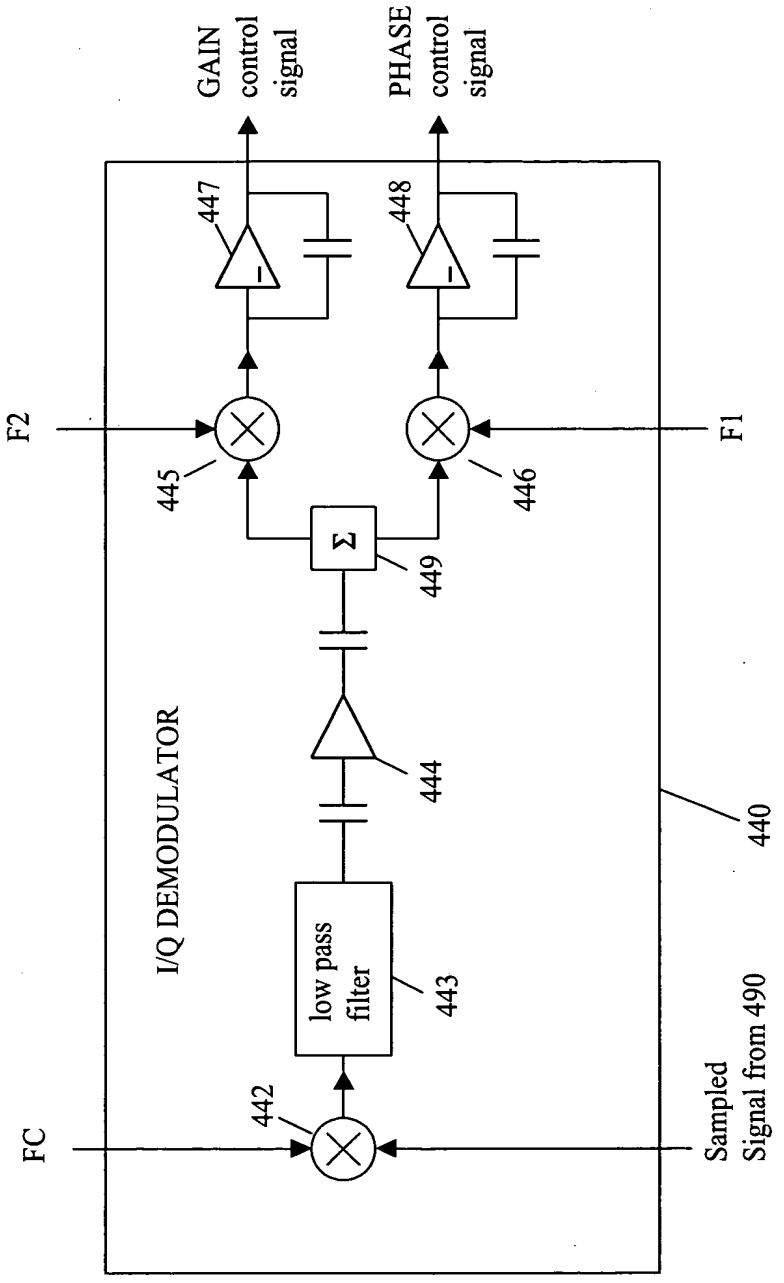

GAIN control signal
PHASE control signal
447
448
F2
F1
445
446
Σ
449
444
I/Q DEMODULATOR
low pass filter
443
440
442
FC
Sampled Signal from 490

FIG. 10

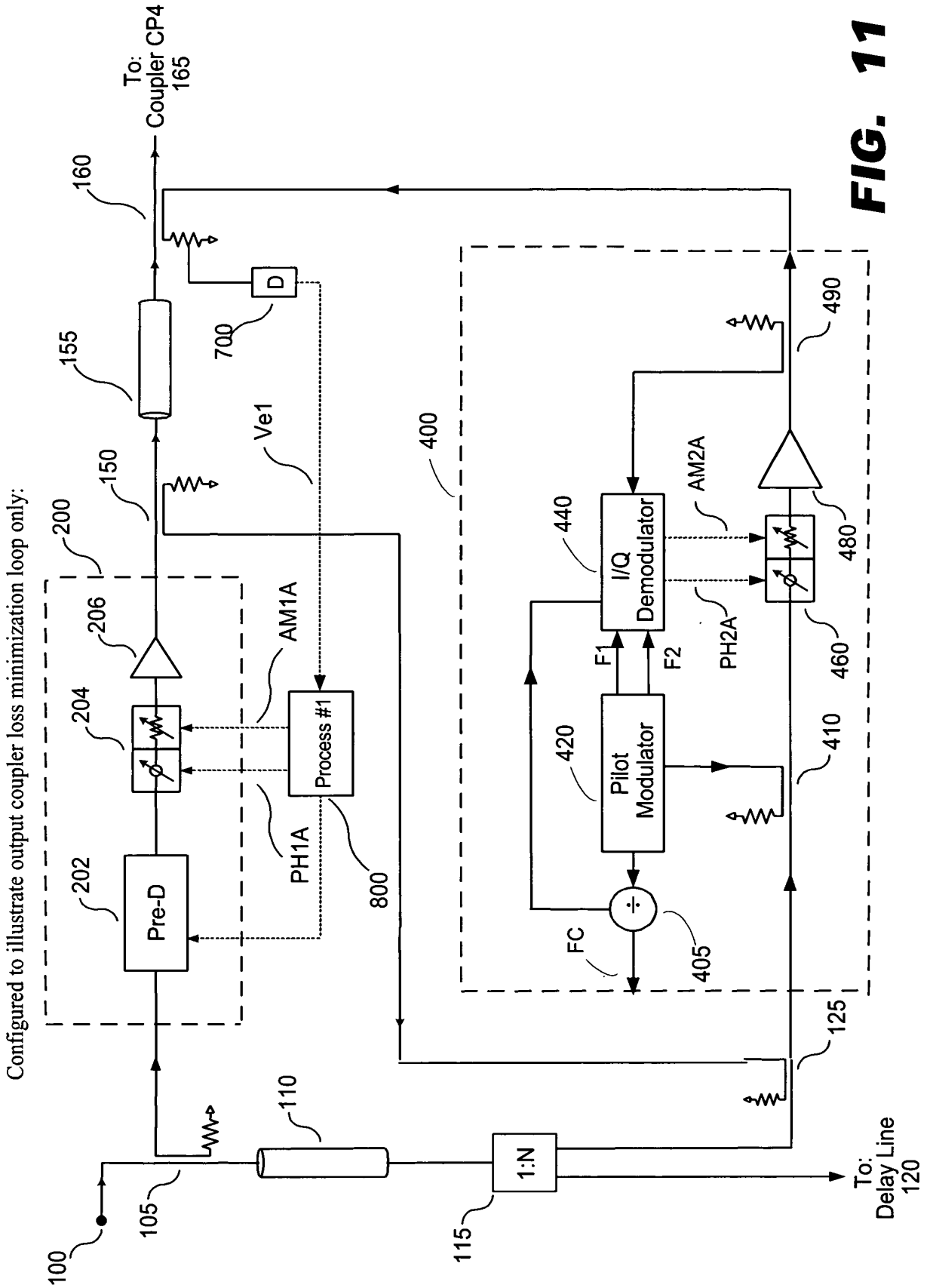

Configured to illustrate output coupler loss minimization loop only:
To: Coupler CP4 165
160
155
700
D
150
Ve1
200
206
AM1A
204
Process #1
PH1A
800
202
Pre-D
100
105
110
115
1:N
125
To: Delay Line 120
400
490
AM2A
440
I/Q Demodulator
480
F1
F2
PH2A
460
420
Pilot Modulator
410
FC
405

FIG. 11

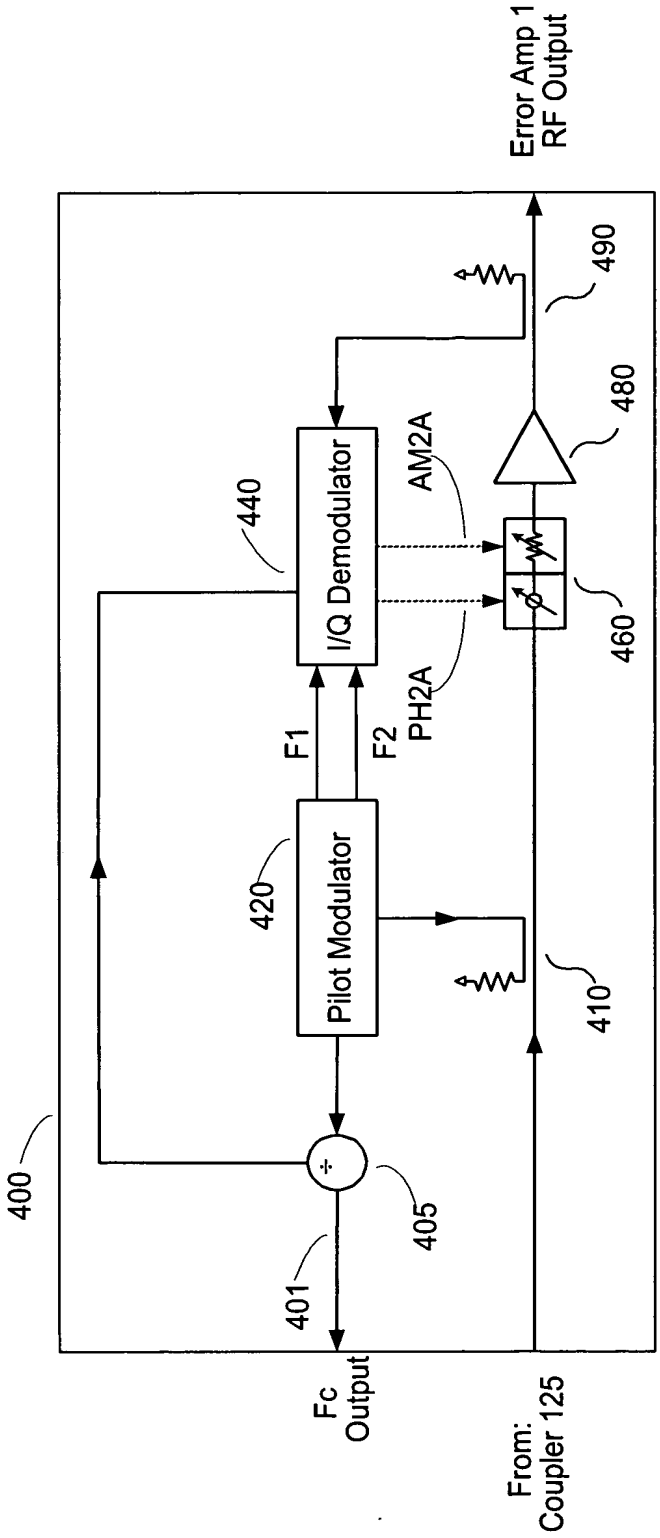

Error Amp 1
RF Output
490
480
AM2A
440
I/Q Demodulator
460
PH2A
F1
F2
420
Pilot Modulator
410
400
405
401
Fc
Output
From:
Coupler 125

FIG. 12

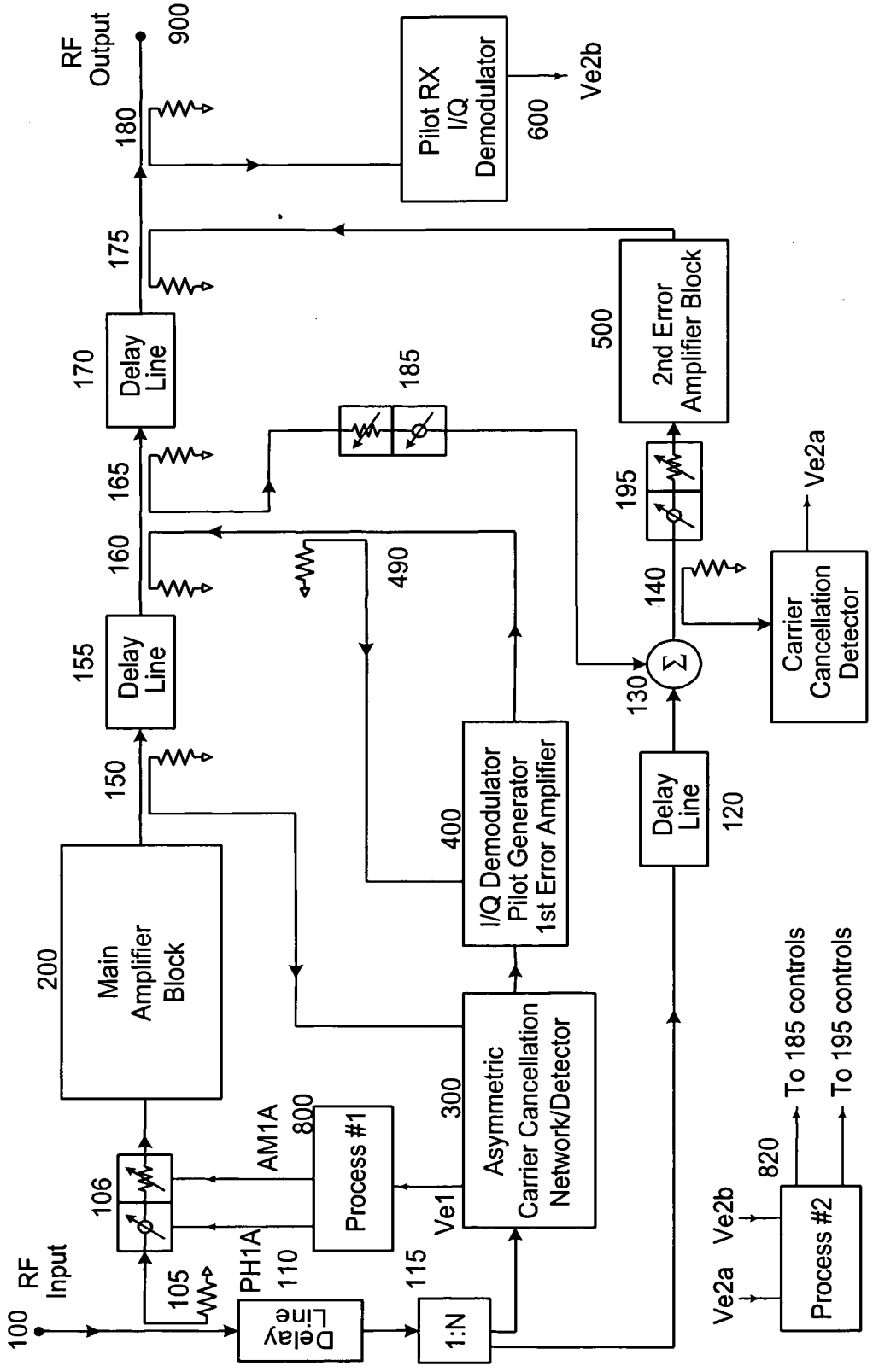

RF Input
100
Delay Line
105
PH1A
110
106
AM1A
800
Process #1
Ve1
115
1:N
300
Asymmetric Carrier Cancellation Network/Detector
200
Main Amplifier Block
150
155
Delay Line
160
165
170
Delay Line
175
180
RF Output
900
185
490
400
I/Q Demodulator Pilot Generator 1st Error Amplifier
Pilot RX I/Q Demodulator
600
Ve2b
500
2nd Error Amplifier Block
195
140
130
Σ
Delay Line
120
Carrier Cancellation Detector
720
Ve2a
Ve2b
Ve2a
820
Process #2
To 185 controls
To 195 controls

FIG. 13A

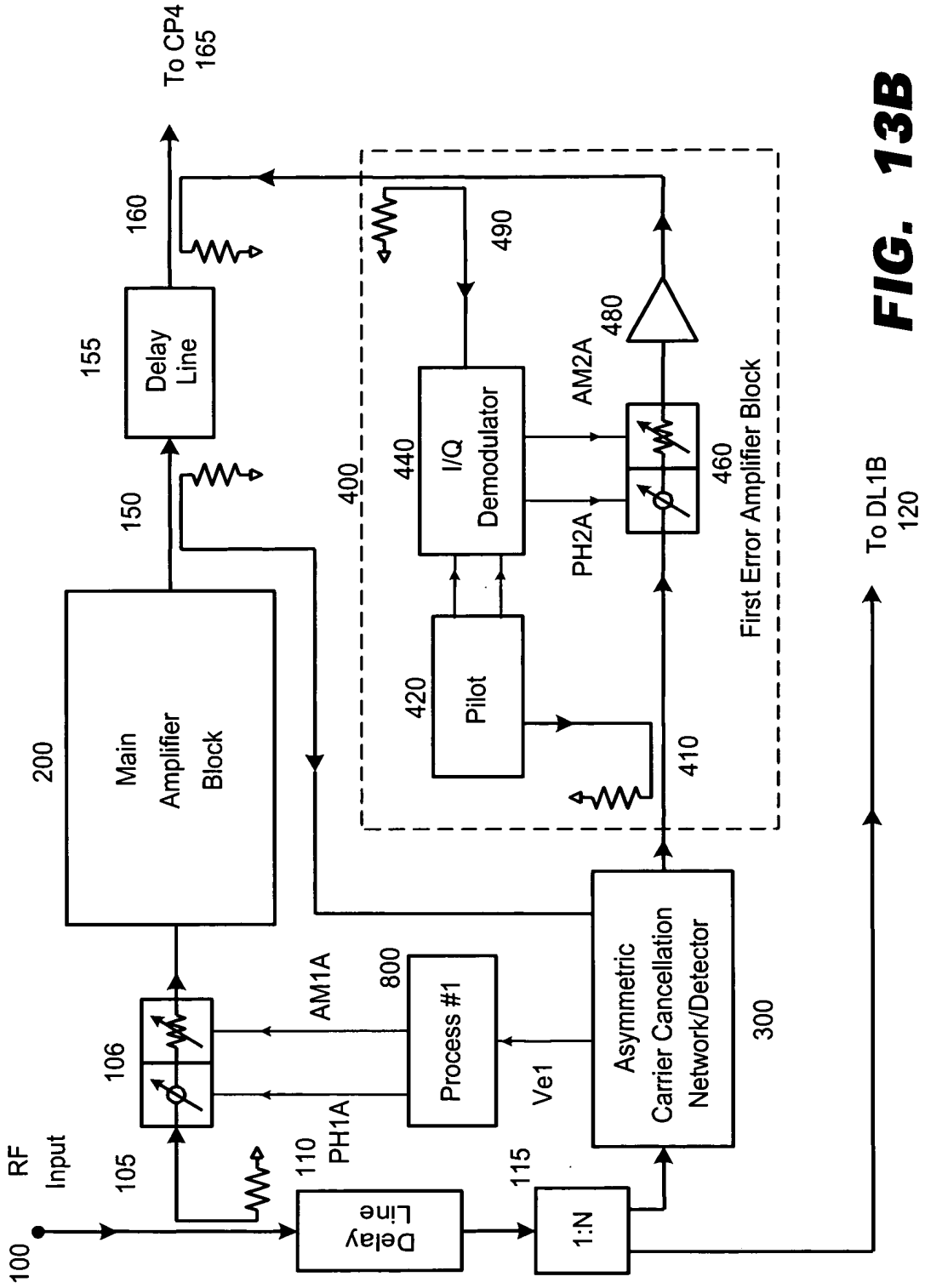

100
RF Input
105
106
110
PH1A
AM1A
800
Process #1
Ve1
115
1:N
Delay Line
Asymmetric Carrier Cancellation Network/Detector
300
To DL1B 120
200
Main Amplifier Block
150
155
Delay Line
160
To CP4 165
400
First Error Amplifier Block
410
420
Pilot
440
I/Q Demodulator
PH2A
AM2A
460
480
490

FIG. 13B

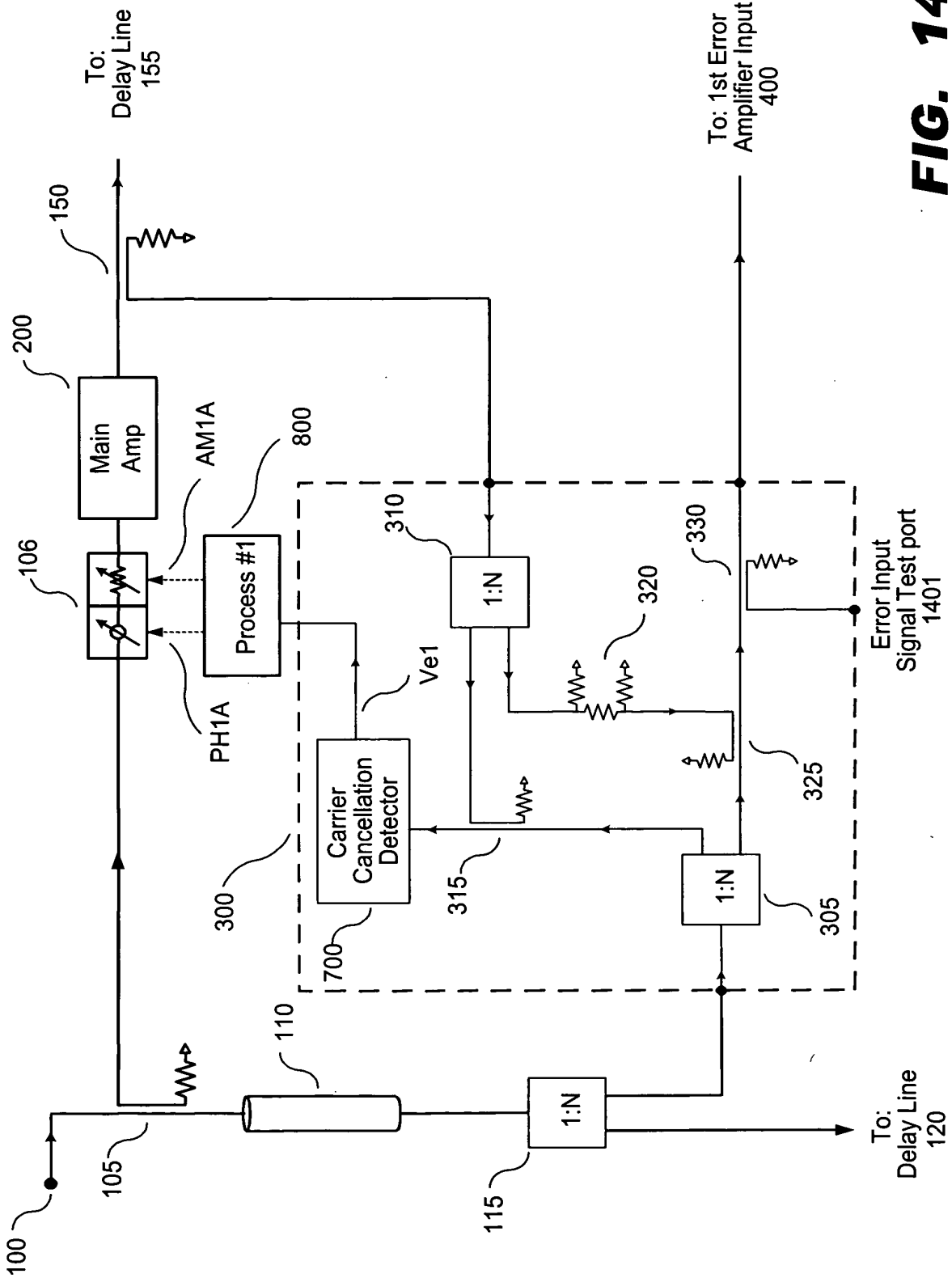

To:
Delay Line
155
150
200
Main
Amp
AM1A
800
106
Process #1
PH1A
310
1:N
330
320
Ve1
Carrier
Cancellation
Detector
300
315
700
325
1:N
305
110
1:N
115
105
100
To: 1st Error
Amplifier Input
400
Error Input
Signal Test port
1401
To:
Delay Line
120

FIG. 14

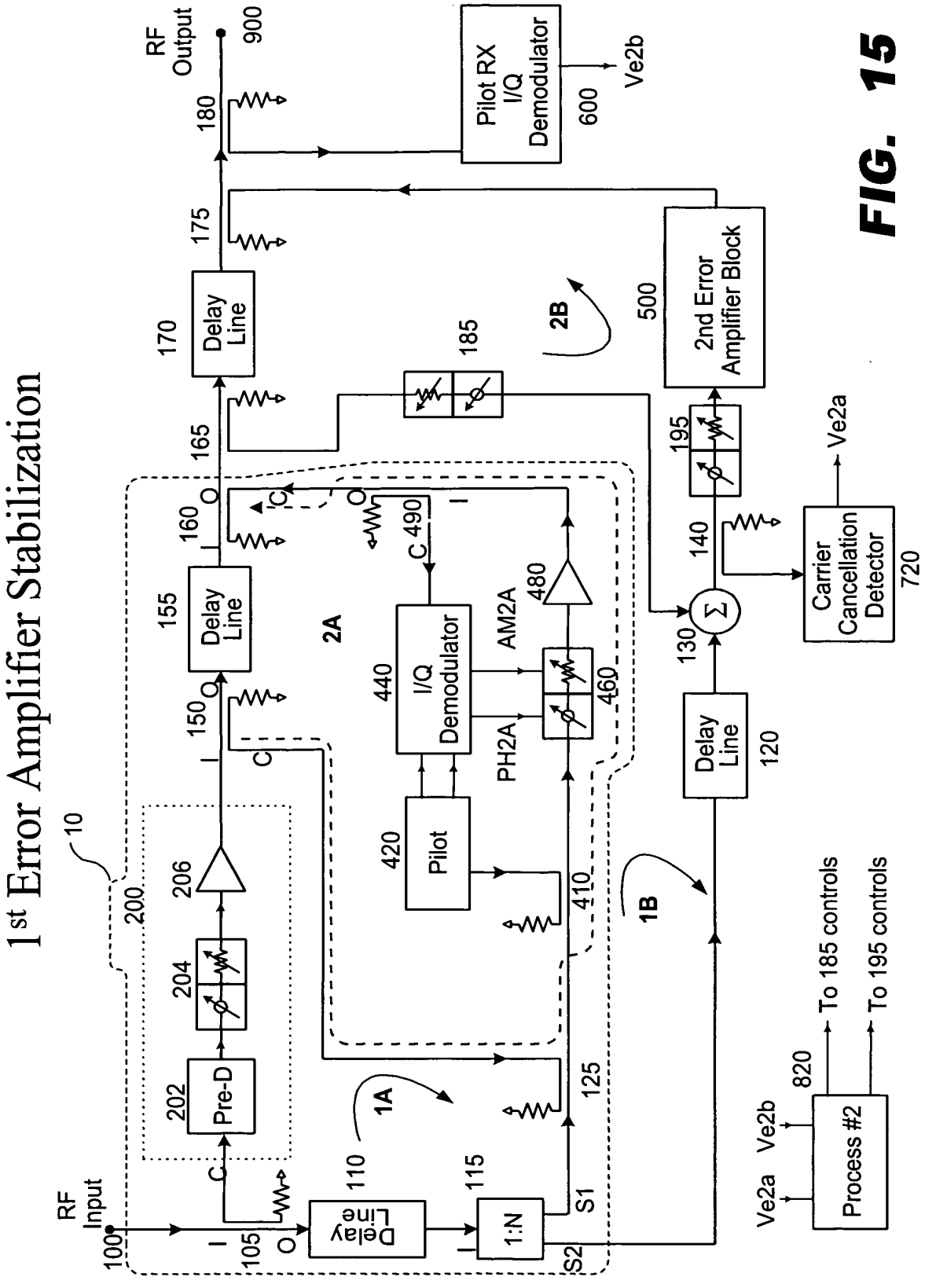

1st Error Amplifier Stabilization
RF Input
100
RF Output
900
10
200
202
Pre-D
204
206
105
110
Delay Line
115
1:N
S1
S2
125
1A
1B
2A
2B
120
Delay Line
130
140
150
155
Delay Line
160
165
170
Delay Line
175
180
185
195
420
Pilot
440
I/Q Demodulator
AM2A
PH2A
460
480
490
410
500
2nd Error Amplifier Block
600
Pilot RX I/Q Demodulator
Ve2b
720
Carrier Cancellation Detector
Ve2a
820
Process #2
To 185 controls
To 195 controls

FIG. 15

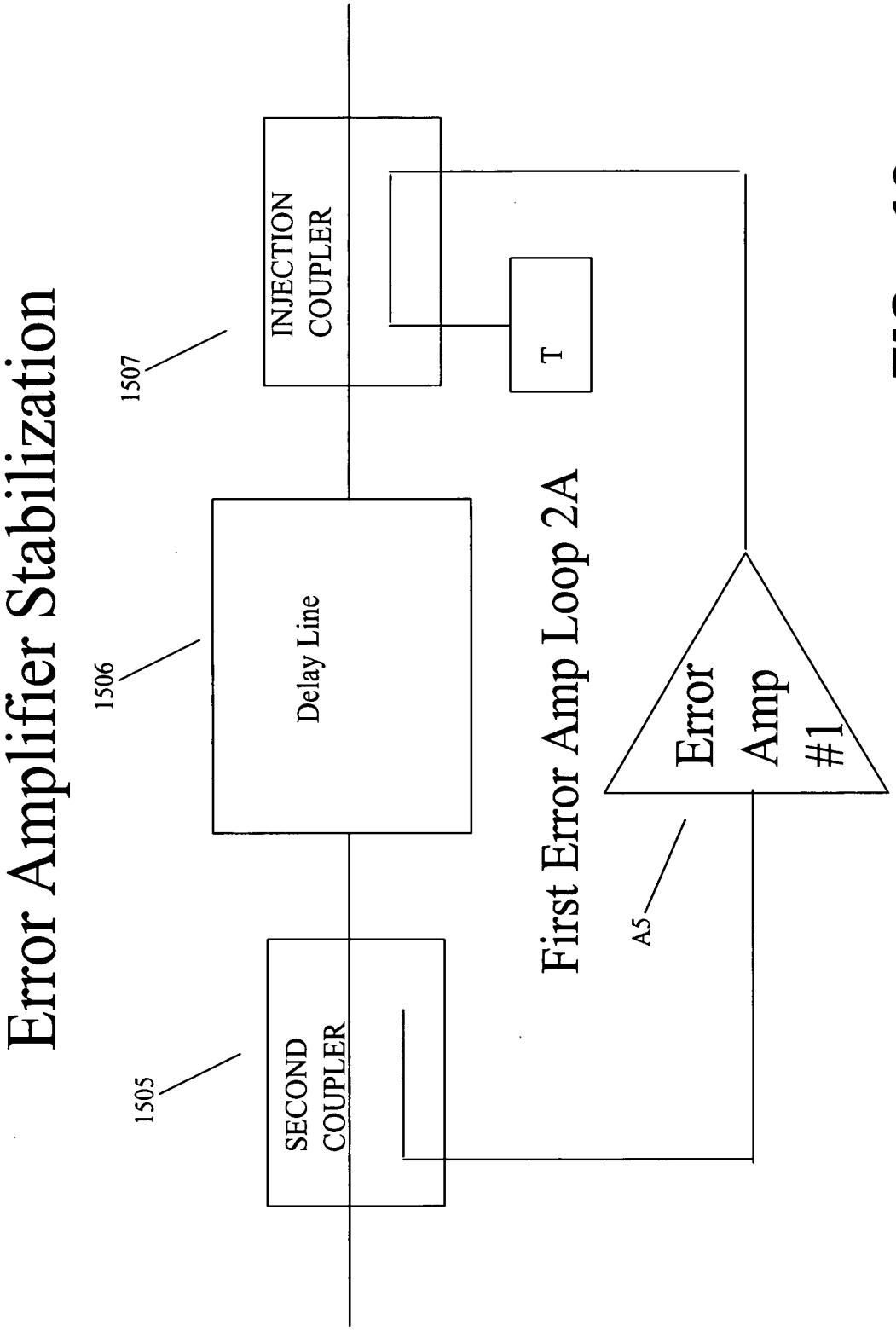

Error Amplifier Stabilization
1507
INJECTION COUPLER
T
1506
Delay Line
First Error Amp Loop 2A
Error Amp #1
A5
1505
SECOND COUPLER

FIG. 16

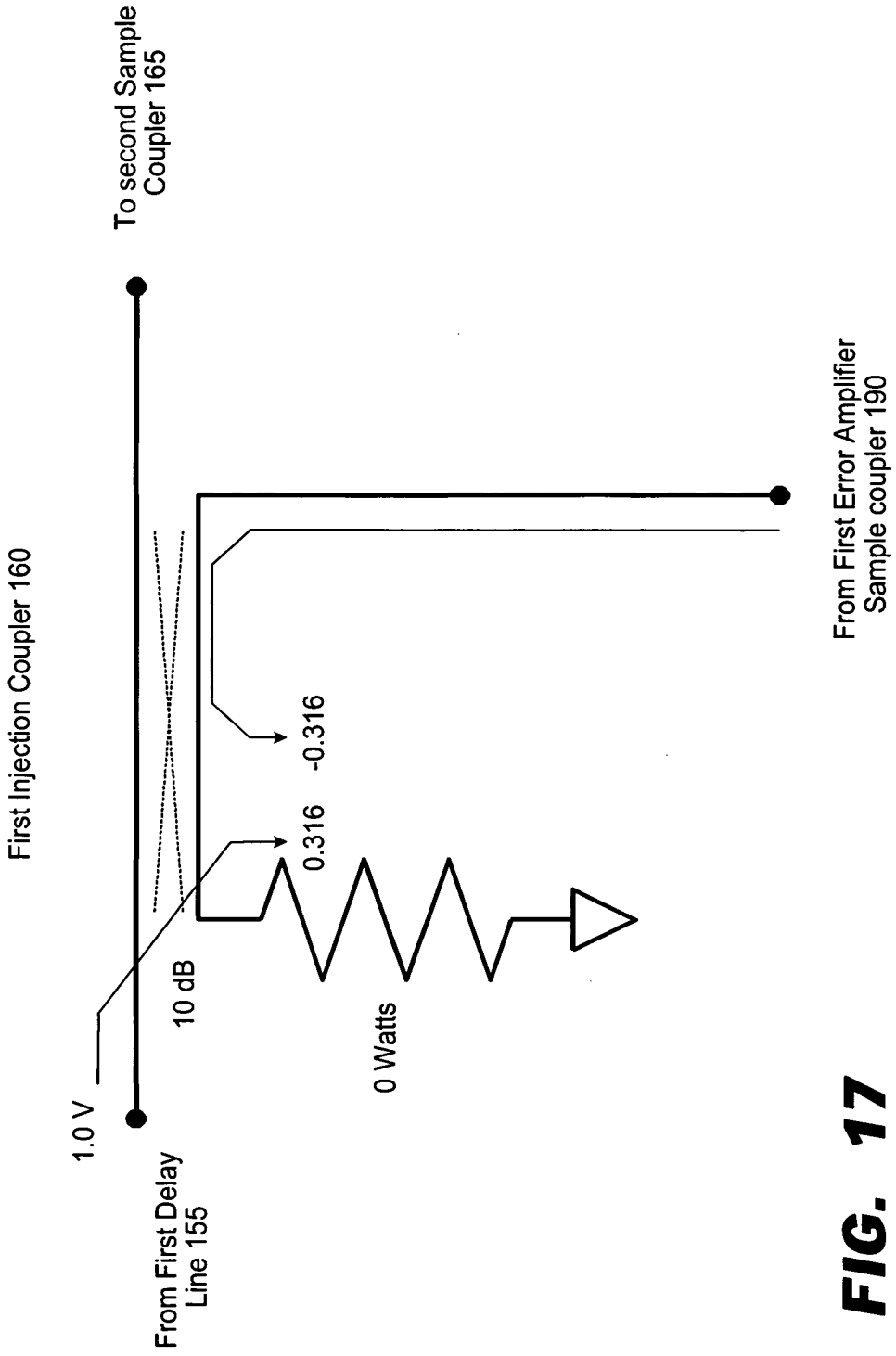

First Injection Coupler 160
To second Sample Coupler 165
From First Error Amplifier Sample coupler 190
From First Delay Line 155
1.0 V
10 dB
0.316
-0.316
0 Watts

FIG. 17

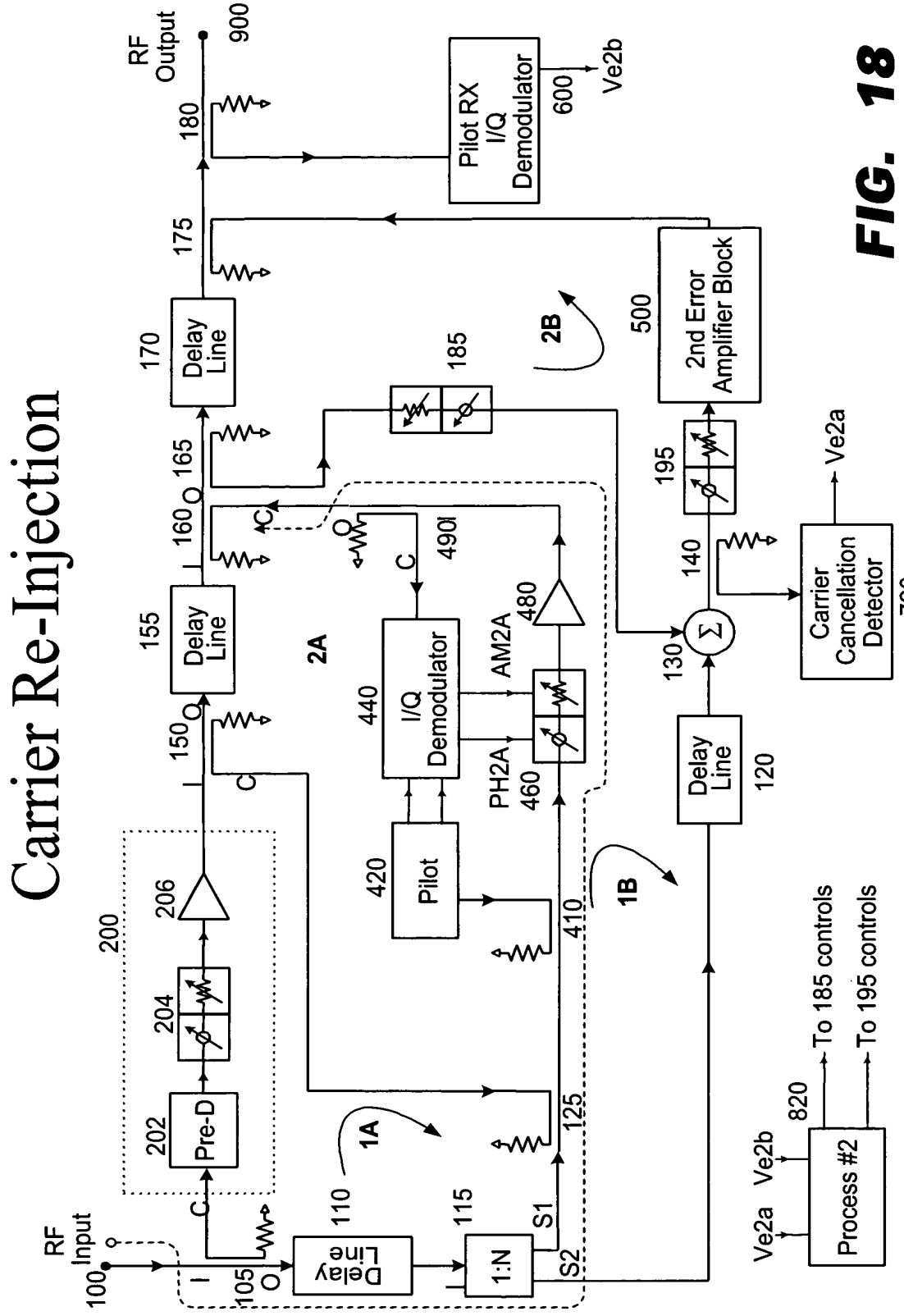

Carrier Re-Injection
RF Input
100
105
I
O
C
200
202
Pre-D
204
206
110
Delay Line
115
1:N
S1
S2
125
1A
150
155
160
165
170
175
180
RF Output
900
Delay Line
Delay Line
Delay Line
2A
2B
1B
185
490
440
I/Q Demodulator
AM2A
PH2A
480
460
420
Pilot
410
130
140
120
195
500
2nd Error Amplifier Block
Pilot RX I/Q Demodulator
600
Ve2b
Carrier Cancellation Detector
720
Ve2a
Ve2a
Ve2b
820
Process #2
To 185 controls
To 195 controls

FIG. 18

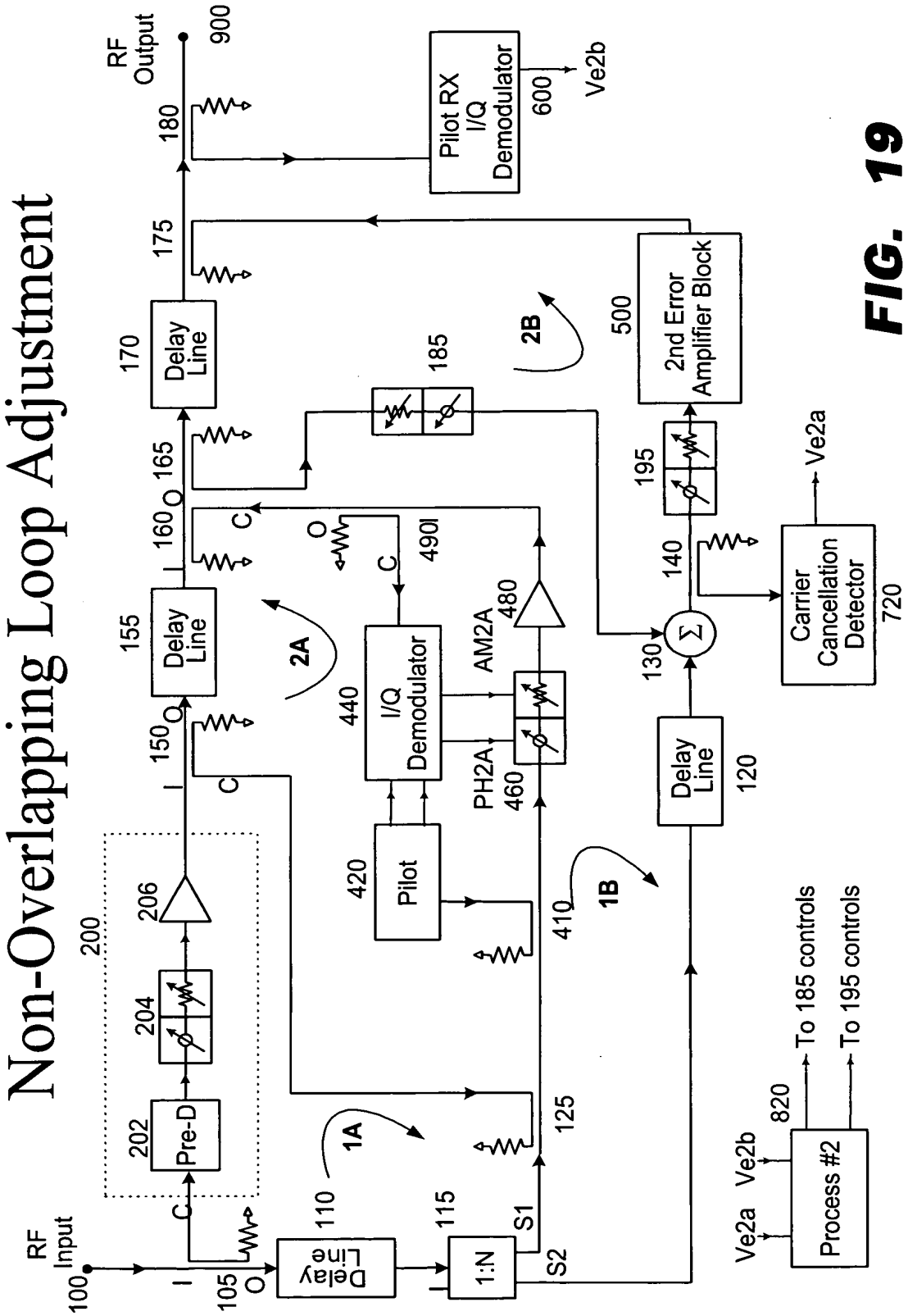

Non-Overlapping Loop Adjustment
RF Input
100
105
110
115
Delay Line
1:N
S1
S2
125
200
202
Pre-D
204
206
150
155
160
165
170
175
180
RF Output
900
Delay Line
Delay Line
Delay Line
1A
2A
2B
1B
410
420
Pilot
440
I/Q Demodulator
460
PH2A
480
AM2A
490I
185
130
140
195
500
2nd Error Amplifier Block
Pilot RX I/Q Demodulator
600
Ve2b
Carrier Cancellation Detector
720
Ve2a
120
Ve2a
Ve2b
820
Process #2
To 185 controls
To 195 controls

FIG. 19